AMC and FMC Modules

Data Sheets of TEWS’ AMC and FMC Modules
About TEWS TECHNOLOGIES

TEWS TECHNOLOGIES is a leading solutions provider of embedded I/O and CPU products based on open architecture standards such as PMC, XMC, IndustryPack® (IP), CompactPCI, standard PCI, PCIe, VME, AMC, and FMC.

TEWS has more than 40 years of experience designing and building turn-key embedded interface solutions using the philosophy to listen and respond to our customers’ needs.

Using this ‘customer first’ approach, TEWS has developed a large number of standard and custom products for applications in industrial control, telecommunication infrastructure, medical equipment, traffic control and COTS.

TEWS’ line of embedded I/O solutions is available worldwide through a global network of distributors.

Software support

Software support is a critical and defining component of the TEWS’ I/O product offering. Our modular hardware designs are coupled with extensive software drivers and support for most major real-time and server operating systems such as VxWorks, Windows, Integrity, Linux, LynxOS, and QNX. Supported CPU architectures are Intel, PowerPC and 68k (for IndustryPack only).

For IndustryPack carriers and modules, TEWS has developed a layered driver concept that includes both a carrier driver layer and an IP module driver layer.

All TEWS’ IndustryPack carriers are supported directly by the carrier driver, and a generic driver is included for integration of third party products.

A key element of our software is our support staff. All TEWS’ support engineers are professionally trained to ensure in-depth support for software drivers and integration.
Quality Assurance / Warranty

TEWS operates three subsidiaries to meet global demand for pre and post sales support, reduced development time, long term product availability, and complete product lifecycle management.

TEWS is committed to continuously improving the quality of our products and services. As a reflection of our commitment to quality, TEWS has implemented and received ISO9001:2008 certification.

All TEWS’ products feature a five-year limited warranty.

RoHS / WEEE Compliance

TEWS TECHNOLOGIES believes in conducting business in a manner that respects the environment and consequently has embraced the RoHS regulations of the European Community.

Non-compliant products will continue to be available for all applications which are exempt from the RoHS directives and have a continuing requirement for leaded solder.
AMC Modules

Advanced Mezzanine Card (AdvancedMC) AMC is a PCI Industrial Computer Manufacturers Group specification (PICMG AMC.0 and PICMG AMC.x, respectively) for hot-swappable and field-replaceable mezzanine cards.

AdvancedMC represents the industry’s next generation mezzanine standard. In addition to providing hot swap capability, intelligent platform management (IPMI), greater potential power/size, and the other enhancements made possible by AdvancedTCA, AdvancedMC is intended to help customers take advantage of the performance enhancements of new, fast, wide-bandwidth serial buses, including PCI Express.

TEWS Technologies is expanding its industry leading embedded I/O product line to support the next-generation open-architecture standard. With its background and long-term experience in interface products based on IndustryPack, PMC, XMC, CompactPCI, PCI, PCIe, FMC, and VME standards. TEWS is growing its product range with the introduction of AMC (Advanced Mezzanine Card) modules.

AMCs are designed to work on a carrier card (primarily AdvancedTCA) and can also be plugged into a backplane directly as defined by the MicroTCA specification.

Especially the latter offers attractive possibilities for industrial grade COTS systems with improved Reliability, Availability, Serviceability and Performance. If you wish to inquire about custom VME designs, please contact TEWS directly at our offices in Germany or the United States. TEWS works closely with OEM and government customers to deliver accelerated time to market, long-term product availability and comprehensive product lifecycle management -- from the design stage through manufacturing, testing and beyond to post-sales support.

All TEWS modules feature a five-year limited warranty, and many are offered standard in extended temperature (-40°C to +85°C). Software drivers for VxWorks, LynxOS, Linux, QNX, Integrity and Windows are available.

For more information go to www.tews.com.
Application Information

The TAMC002-TM is a standard Mid-Size/Full-Size MTCA.4 compliant Micro Rear Transition Module compatible to the TAMC220.

Two AirmaxVS connectors provide access to all IP I/O lines of the TAMC220. The I/O lines are routed to three VHD68 SCSI-V connectors in the front panel and also to three 50-pin flat cable connectors that may be used for rack internal wiring or laboratory use.

According to MTCA.4, the TAMC002-TM provides an I2C EEPROM, an I2C temperature sensor and an I2C I/O Extender device. The I/O Extender is used to provide various management signals on the µRTM, with the management being handled by the MMC of the TAMC220.

Technical Information

- Form Factor: PICMG MTCA.4 Rear Transition Module
- Board size: Double Mid-Size or Double Full-Size
- MTCA.4 compatible IPMI support
- I/O Connectors:
  - VHD68 SCSI-V (front panel)
  - 50-pol. flat cable
- Front-Panel LEDs:
  - Blue Hot-Swap LED
  - Red Failure LED (LED1)
  - Green Board OK LED (LED2)
- Operating temperature -40°C to +85°C
- MTBF (MIL-HDBK217F/FN2 G6 20°C): 448000h
Order Information

RoHS Compliant
TAMC002-TM-10R  MTCA.4 Rear I/O µRTM for TAMC220, Double Mid-Size, 3 x VHD68
TAMC002-TM-11R  MTCA.4 Rear I/O µRTM for TAMC220, Double Full-Size, 3 x VHD68

For the availability of non-RoHS compliant (leaded solder) products please contact TEWS.

Documentation

Related Products
TA307  Cable Kit for modules with VHD68 connector
Application Information

The TAMC100 is a standard single width Mid-Size/Full-Size AMC.1 (PCI-Express) compliant carrier for one single-size IndustryPack (IP) module used to build modular, flexible and cost effective I/O solutions for applications in process control, medical systems, telecommunication and traffic control. A HD50 SCSI-2 type connector provides access to all IP I/O lines.

The TAMC100 is a versatile solution to upgrade well known legacy I/O solutions to a high performance form factor.

All IP interrupt request lines are mapped to PCIe INTA. Alternatively Message Signaled Interrupts (MSI) can be used. For fast interrupt source detection the TAMC100 provides a special IP interrupt status register.

The IP power lines are fuse protected by self-healing fuses and RF filtered. The operating temperature range is -40°C to +85°C.

According to AMC.0, the TAMC100 provides an IPMI compliant Module Management Controller (MMC) with temperature monitoring and hot-swap support.

The TAMC100 is available as mid-size module or as full-size module.

Please note that the mid-size module has restrictions to its usage because of a component height violation. It is within the responsibility of the user to carefully check if the mid-size module with its component height violation can be used in his system. Otherwise damage of the TAMC100 or its slot to be used in may occur! For more information see the user manual TAMC100-DOC.

Technical Information

- Form Factor: PCIMG AMC.1 Module
  - Board size: 180.6mm x 73.5mm
  - Single width
  - Mid-Size/Full-Size front panel
- Fabric Interface:
  - PCIe single lane (x1) on AMC Port 4 (AMC.1 Type 1 compliant)
- IPMI V1.5 Support
- Front Panel LEDs:
  - Blue Hot-Swap LED
  - Red Fail LED (LED1)
  - Green IP-Activity LED (LED 2)
- ANSI/VITA 4-1995 compliant interface to one IndustryPack module
  - IndustryPack slot: one single-size
  - 8/32 MHz interface, no DMA
  - 8 Mbytes IP memory space
  - Routing of all IP interrupts to PCIe INTA/MSI, local interrupt status register
  - I/O access: HD50 SCSI-2 type connector
- Self-Healing fuses and RF-filtering on all IP power lines
- Operating temperature: -40°C to +85°C
- MTBF (MIL-HDBK217F/FN2 Gb 20°C): 633.000 h

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Order Information

RoHS Compliant
TAMC100-10R  1 Slot IndustryPack Carrier, Single Mid-Size *)
TAMC100-11R  1 Slot IndustryPack Carrier, Single Full-Size

*) Please note that the mid-size module has restrictions to its usage because of a component height violation. It is within the responsibility of the user to carefully check if the mid-size module with its component height violation can be used in his system. Otherwise damage of the TAMC100 or its slot to be used in may occur! For more information see the user manual TAMC100-DOC

For the availability of non-RoHS compliant (leaded solder) products please contact TEWS.

Documentation
TAMC100-DOC  User Manual

Software
CARRIER-SW-25  Integrity Software Support
CARRIER-SW-42  VxWorks Software Support (Legacy and VxBus-enabled Software Support)
CARRIER-SW-65  Windows Software Support
CARRIER-SW-72  LynxOS Software Support
CARRIER-SW-82  Linux Software Support
CARRIER-SW-95  QNX Software Support

For other operating systems please contact TEWS.

Related Products
TA301  Cable Kit for Modules with HD50 Connector
**Application Information**

The TAMC200 is a standard double Mid-Size/Full-Size AMC.1 (PCI-Express) compliant carrier for up to three single-size or one double-size and one single-size IndustryPack (IP) modules used to build modular, flexible and cost effective I/O solutions for all kinds of applications like process control, medical systems, telecommunication and traffic control. Three VHD68 SCSI-V (VHDCI/Champ) type connectors provide access to all IP I/O lines.

The TAMC200 is a versatile solution to upgrade well known legacy I/O solutions to a high performance form factor.

All IP interrupt request lines are mapped to PCIe INTA, alternatively Message Signaled Interrupts (MSI) can be used. For fast interrupt source detection the TAMC200 provides a special IP interrupt status register.

The IP power lines are fuse protected by self-healing fuses and RF filtered. The operating temperature range is -40°C to +85°C.

According to AMC.0, the TAMC200 provides an IPMI compliant Module Management Controller (MMC) with temperature monitoring and hot-swap support.

**Technical Information**

- **Form Factor:** PCIMG AMC.1 Module
- **Board size:** 180.6mm x 146.5mm
- **Double Mid-Size or Full-Size front panel
- **Fabric Interface:**
  - PCIe single lane (x1) on AMC Port 4 (AMC.1 Type 1 compliant)
- **IPMI V1.5 Support**
- **Front Panel LEDs:**
  - Blue Hot-Swap LED
  - Red Fail LED (LED1)
  - Green Power Good / Activity LED (LED 2)
- **ANSI/VITA 4-1995 compliant interface to three IndustryPack modules**
- **3 IndustryPack slots:** three single-size IPs or one single-size and one double-size IP
- **8/32 MHz interface, no DMA**
- **8 Mbytes memory space per IP Slot**
- **Routing of all IP interrupts to PCIe INTA/MSI, local interrupt status register**
- **I/O access:** VHD68 SCSI-V (VHDCI/Champ) type connector per IP
- **Self-Healing fuses and RF-filtering on all IP power lines**
- **Operating temperature:** -40°C to +85°C
- **MTBF (MIL-HDBK217F/FN2 Gb 20°C):** 250,000 h
The Embedded I/O Company

Order Information

RoHS Compliant
TAMC200-10R 3 Slot IndustryPack Carrier, Double Mid-Size*)
TAMC200-11R 3 Slot IndustryPack Carrier, Double Full-Size

*) Please note that the mid-size module has restrictions to its usage because of a component height violation. It is within the responsibility of the user to carefully check if the mid-size module with its component height violation can be used in his system. Otherwise damage of the TAMC200 or its slot to be used in may occur! For more information see the user manual TAMC200-DOC

For the availability of non-RoHS compliant (leaded solder) products please contact TEWS.

Documentation
TAMC200-DOC User Manual

Software
CARRIER-SW-25 Integrity Software Support
CARRIER-SW-42 VxWorks Software Support (Legacy and VxBus-enabled Software Support)
CARRIER-SW-65 Windows Software Support
CARRIER-SW-72 LynxOS Software Support
CARRIER-SW-82 Linux Software Support
CARRIER-SW-95 QNX Software Support

For other operating systems please contact TEWS.

Related Products
TA307 Cable Kit for Modules with VHD68 Connector

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The Embedded I/O Company

TAMC220 3 Slot IndustryPack® Carrier for MTCA.4 Rear-I/O

Application Information
The TAMC220 is a standard double Mid-Size/Full-Size AMC.1 (PCI-Express) and MTCA.4 compliant carrier for up to three single-size, or one double-size and one single-size IndustryPack (IP) modules. It can be used to build modular, flexible and cost effective I/O solutions for all kinds of applications like process control, medical systems, telecommunication and traffic control. The TAMC220 is a versatile solution to upgrade well known legacy I/O solutions to a high performance form factor.

Two AirMaxVS™ connectors provide access to all IP I/O lines via a compatible µRTM, such as the TAMC002-TM. The IP power lines are protected by self-healing fuses and are RF filtered. The operating temperature range is -40°C to +85°C.

According to AMC.0, the TAMC220 provides an IPMI compliant Module Management Controller (MMC) with temperature monitoring and hot-swap support.

The TAMC220 is available as a mid-size module or as a full-size module.

TCLKA and TCLKB are connected to the µRTM via M-LVDS transceivers. Both signals can be used as bi-directional single-ended signals.

Technical Information
- Form Factor: PICMG MTCA.4 Module
- Board size: Double Mid-Size or Double Full-Size
- PCIe x1 Port (AMC.1 Type 1 compliant)
- IPMI V1.5 support
- Front-Panel LEDs:
  - Blue Hot-Swap LED
  - Red Failure LED (LED1)
  - Green Board OK/Activity LED (LED2)
  - Green ACKNOWLEDGE LED for each IP slot
- ANSI/VITA 4-1995 compliant interface to three IndustryPack modules
- 3 IndustryPack slots: three Single-Size IPs or one Single-Size and one Double-Size IP
- 8/32 MHz interface, no DMA
- 8 Mbytes memory space per IP Slot
- Routing of all IP interrupts to PCIe INTA/MSI, local interrupt status register
- Rear-I/O access to all 150 IP I/O lines via AirmaxVS™ 90-pos connectors to a compatible RTM (for example, TAMC002-TM)
- Self Healing fuses and RF-filtering on all IP power lines
- Operating temperature -40°C to +85°C
- MTBF (MIL-HDBK217F/FN2 G0 20°C) TAMC220-xxR: 268000h

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**Order Information**

**RoHS Compliant**
- TAMC220-10R: 3 Slot IndustryPack Carrier, Double Mid-Size, MTCA.4 Rear I/O*
- TAMC220-11R: 3 Slot IndustryPack Carrier, Double Full-Size, MTCA.4 Rear I/O

*) Please note that the mid-size module has restrictions to its usage because of a component height violation. It is within the responsibility of the user to carefully check if the mid-size module with its component height violation can be used in his system. Otherwise damage of the TAMC220 or its slot to be used in may occur! For more information see the user manual TAMC220-DOC.

For the availability of non-RoHS compliant (lead solder) products please contact TEWS.

**Documentation**

**Software**
- CARRIER-SW-25: Integrity Software Support
- CARRIER-SW-42: VxWorks Software Support (Legacy and VxBus-Enabled Software Support)
- CARRIER-SW-65: Windows Software Support
- CARRIER-SW-72: LynxOS Software Support
- CARRIER-SW-82: Linux Software Support
- CARRIER-SW-95: QNX Software Support

For other operating systems please contact TEWS.

**Related Products**
- TAMC002-TM: MTCA.4 Rear I/O µRTM for TAMC220, 3 x VHD6

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Application Information

The TAMC260 is a standard Mid-Size/Full-Size AMC module that provides one slot for a single-width PMC module used to build modular, flexible and cost effective I/O solutions for applications in process control, medical systems, telecommunication and traffic control.

32 bit PCI accesses are supported on PCI bus with PCI frequency 33 MHz and also 66 MHz. The PLX8112 PCIe-to-PCI bridge provides the real connection between primary PCIe link and the secondary PMC slot. The bridge controls all PCI accesses and the frequency for the PMC access.

The TAMC260 supports front panel I/O, alternatively a 68 pin SCSI-V type connector provides access to the PMC P14 back I/O lines.

The TAMC260 is a versatile solution to upgrade well known legacy I/O solutions to a high performance form factor.

According to AMC.0, the TAMC260 provides an IPMI compliant Module Management Controller (MMC) with temperature monitoring and hot-swap support.

Technical Information

- Form Factor: PICMG AMC.1 Module
- Board size: 180.6 mm x 146.5 mm
- Double-width / Mid-Size or Full-Size
- PCIe single lane (1x) port (AMC.1 Type 1 compliant)
- IPMI support
- Front Panel LEDs:
  - Blue Hot-Swap LED
  - Red Power Good LED (LED1)
  - Green PMC-Present LED (LED2)
- One PMC site conforming to PMC standard (IEEE 1386.1)
- Front panel I/O
- P14 back I/O via a 68 pin SCSI-V type connector
- PCI 3.0 compliant interface
- PCI Interface: 33/66 MHz; 32 bit
- 5V and 3.3V PCI I/O signaling voltage possible
- Operating temperature -40°C to +85°C
Order Information

RoHS Compliant

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<td>1 Slot PMC Carrier, Double Mid-Size, 32 bit, 33/66 MHz, 3.3V PCI I/O signaling voltage, PCIe x1</td>
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For the availability of non-RoHS compliant (leaded solder) products please contact TEWS.

Documentation

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Related Products

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Application Information

The TAMC532 is an Advanced Mezzanine Card (AMC) according to MTCA.4 (MicroTCA Enhancements for Rear I/O and Precision Timing). 32 analog input channels allow sampling of analog signals with 75 Msps at 12 Bit resolution (optional 50 Msps at 14 Bit).

The TAMC532 utilizes Back-I/O via Zone 3 to interface the ADCs with the signal conditioning located on the µRTM. This modular concept allows adapting the TAMC532 to nearly any analog input requirement without changing the AMC itself.

A very powerful on-board clocking structure enables using the TAMC532 in nearly all kind of clocking scenarios. A self-clocked application as well as synchronizing multiple TAMC532 is possible, allowing applications with up to several hundred simultaneous sampled channels.

Data readout can be done via several interfaces like e.g. PCI-Express or two SFP-cages in the front panel.

The on-board DRR3 memory can be used for data buffering in triggered applications that require subsequent readout. Assuming sufficient data fabric bandwidth, the DDR3 memory can also be used as double buffer, allowing infinite data acquisition.

Up to eight backplane triggers are available, each configurable as input or output.

The TAMC532 is equipped with a powerful Kintex-7 FPGA for data preprocessing and transfer. By default, the Kintex-7 FPGA is configured with a firmware that provides a very functional readout system and full control over the numerous clocking and trigger options. It can also be adapted to customer needs if necessary.

In-circuit programming and debugging of the FPGA design (e.g. using Xilinx “ChipScope”) is supported. The Program and Debug Box TA900 or the standard Xilinx JTAG header allows access to the module while it is inserted in a system. In addition to the module’s JTAG Chain, the TA900 allows access to the UART of the on-board Module Management Controller (MMC) and to two user pins of the FPGA. If a UART core is implemented in the FPGA, serial communication via the TA900 is possible.

The TA900 can be accessed by USB 2.0 and by a 14-pin JTAG Header (e.g. for connecting a Xilinx Platform Cable).
Technical Information

- Form Factor: PICMG MTCA.4 module
  - Board size: 180.6 mm x 146.5 mm
  - Double-width / Mid-Size
- Fabric Interconnects
  - Gigabit Ethernet on AMC Port 0
  - x4 PCIe Gen 2 Link (AMC.1 Type 4 compliant)
  - AMC Port 12
  - x1 Link to µRTM
- 2 x SFP+ Cage
- TCLK A and B support
- M-LVDS Transceivers on AMC ports 17-20
- Kintex-7 70T FPGA
  - Integrated PCIe Gen 2 Endpoint Block
  - Multi-Gigabit transceiver with up to 6.6Gb/sec
  - Dual FPGA Configuration Flash
- 2x DDR3 memory
  - 32 bit data bus width each
  - 256 MByte each
- Low Jitter Clock distribution and generation
- 32 x ADC
  - 12 Bit at 75 Msp/s (TAMC532-10R)
  - 14 Bit at 50 Msp/s (TAMC532-11R)
  - ±1V differential analog inputs via Zone 3
- IPMI V1.5 support
- Front Panel LEDs:
  - Blue Hot-Swap LED
  - Red Fail LED
  - Green User LED
- MTCA.4 Zone 3 Interface according to Class A2.1
Order Information

RoHS Compliant
TAMC532-10R Kintex-7 70T, 2 x 256 MByte at 32 Bit DDR3, 32 x 12 Bit 75 Msps ADC
TAMC532-11R Kintex-7 70T, 2 x 256 MByte at 32 Bit DDR3, 32 x 14 Bit 50 Msps ADC

Optional available on request:
- Operating temperature -40°C to +85°C
- Faster FPGA speed grades
- Other FPGA logic densities:
  - Kintex-7 160T
  - Kintex-7 325T
  - Kintex-7 410T
- Memory options:
  - Kintex-7 70T: 2 x 512 MByte at 32 Bit / 2 x 1 GByte at 32 Bit
  - Kintex-7 160T / 325T / 410T: 2 x 1 GByte at 64 Bit / 2 x 2 GByte at 64 Bit

For the availability of non-RoHS compliant (leaded solder) products please contact TEWS.

Documentation
TAMC532-DOC User Manual

Software
TAMC532-SW-25 Integrity Software Support
TAMC532-SW-42 VxWorks Software Support
TAMC532-SW-65 Windows Software Support
TAMC532-SW-72 LynxOS Software Support
TAMC532-SW-82 Linux Software Support
TAMC532-SW-95 QNX Software Support

For other operating systems please contact TEWS.

Related Products
TAMC532-TM-10R µRTM for TAMC532

Accessories
TA900-10R Program and Debug Box, USB, JTAG, 20pin FPC connector, including USB A-USB B and FPC Flexcable
Application Information

The TAMC532-TM is a MTCA.4 compliant Micro Rear Transition Module for the TAMC532. Eight RJ45 connectors are used as input connectors for the 32 differential analog inputs of the TAMC532 TM. Each of the 32 differential analog inputs is connected to its own filter block.

The filter block consists of an input Buffer with programmable gain, a Gaussian shaping amplifier with programmable shaping time and an output buffer with adjustable baseline shift. The Pole-Zero compensation is adjustable by use of a digital potentiometer. This is ideal for readout of charge sensitive preamplifiers.

The baseline shift is useful if the input signal is always positive (or negative). It allows to increase the gain and to make better use of the ADC input voltage range.

All settings are common for groups of 8 inputs.

The output of the filter block is accessible by the AMC via Zone 3. A Clock input is available in the TAMC532-TM front panel as well. A coaxial connector is used to feed the single-ended signal into the TAMC532-TM. After a single-ended to LVDS conversion, the signal is connected to Zone 3, RTM_CLK0.

Zone 3 pin assignment and the µRTM management implementation are MTCA.4 compliant and comply with Zone 3 Classification Recommendation according to Class A2.1.
The Embedded I/O Company

Technical Information

- Form Factor: PICMG MTCA.4 Rear Transition Module
  - Board size: Double Mid-Size
- 32 Analog Input Channels
  - Input connectors: 8 x RJ45
  - Differential input signals
  - Individual filter block for each channel
    - Selectable gain (1, 2, 5, 10)
    - Selectable shaping time (100ns, 1µs, 10µs)
    - Adjustable pole-zero compensation (256 Tap Potentiometer)
  - Adjustable baseline shift (12 Bit DAC)
- Management
  - MTCA.4 compatible IPMI support
  - According to Class A2.1
- Front Panel LEDs:
  - Blue Hot-Swap LED
  - Red Fail LED
  - Green User LED
- MTCA.4 Zone 3 pin assignment according to Class A2.1

Order Information

RoHS Compliant
TAMC532-TM-10R  32 x Analog-In MTCA.4 µRTM for Class A2.1

Documentation
TAMC532-DOC  User Manual

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The TAMC631 is a standard single Mid-Size or Full-Size AMC.1 Type 1 module providing a user configurable XC6SLX25T-2, XC6SLX75T-2, XC6SLX100T-2 or XC6SLX150T-2 Spartan-6 FPGA. The Spartan-6’s PCIe Endpoint Block is connected to AMC port 4. The TAMC631 variants with XC6SLX75T, XC6SLX100T and XC6SLX150T FPGA also provide connections to AMC port 0 and 1.

For flexible front I/O solutions the TAMC631 provides a VITA 57.1 FMC Module slot with a low-pin count connector, allowing active and passive signal conditioning. All FMC I/O lines are directly connected to the FPGA, which maintains the flexibility of the SelectIO technology of the Spartan-6 FPGA. The low-pin count interface includes one multi-gigabit link.

The FPGA is connected to two banks of 128 Mbytes, 16 bit wide DDR3 SDRAM. The SDRAM-interface uses the hardwired internal Memory Controller Blocks of the Spartan-6.

The FPGA is configured by a platform flash which is programmable via a JTAG header. The JTAG header also supports readback and on-chip debuggin of the FPGA design (using Xilinx “ChipScope”). An SPI-EEPROM can be used as alternative configuration source or for user data storage. The TAMC631 is delivered with blank configuration devices.

A programmable clock generator (5 KHz – 500 MHz) supplies up to three different clock frequencies to the FPGA. The clock generator settings are programmable via JTAG and are stored in an EEPROM. In addition two differential reference clocks are available from the FMC slot to the FPGA.

User applications for the TAMC631 with XC6SLX25T-2 and XC6SLX75T-2 FPGA can be developed using the design software ISE WebPACK which can be downloaded free of charge from www.xilinx.com. The larger FPGA densities require a full licensed ISE Design Suite.

The Engineering Documentation TAMC631-ED includes all information needed for customer specific FPGA programming. The FPGA Development Kit TAMC631-FDK includes the engineering documentation, ucf-files with all necessary pin assignments and basic timing constraints, and a well-documented VHDL example application. This example application is called TPLD001 (Tews Programmable Logic Design) and covers the main functionalities of the TAMC631 like DMA capable PCIe endpoint with interrupt support, register mapping, DDR3 memory access and basic I/O to the FMC slot. It comes as a Xilinx ISE project with source code and as a ready-to-download bitstream. It is the basis for fast and reliable customer application development, and can significantly reduce time to market.

Software support for the TPLD001 is available for all major operating systems.

Please note: The TPLD001 requires the Embedded Development Kit (EDK), which is part of the Embedded or System Edition of the ISE Design Suite from Xilinx (downloadable from www.xilinx.com, a 30 day evaluation license is available).

In-circuit programming and debugging of the FPGA design (e.g. using Xilinx “ChipScope”) is supported. The Program and Debug Box TA900 allows access to the module while it is inserted in a system. It provides access to the module’s JTAG Chain, the UART of the on-board Module Management Controller (MMC) and to two user pins of the Spartan-6 FPGA. If a UART core is implemented in the FPGA, serial communication via the TA900 is possible.

The TA900 can be accessed by USB 2.0 and by a 14-pin JTAG Header (e.g. for connecting a Xilinx Platform Cable).

For First-Time-Buyers the TA900 and the TAMC631-ED or TAMC631-FDK is recommended.
The Embedded I/O Company

Technical Information

- Form Factor: PICMG AMC.0 R2.0 Module
  - Board size: 180.6 mm x 73.5 mm
  - Single width
  - Mid-Size or Full-Size front panel
- PCIe x1 port (AMC.1 Type 1 compliant)
  - Optional connection to AMC port 0 & 1 (not for XC6SLX25T)
- IPMI V1.5 support
- Front Panel LEDs:
  - Blue Hot-Swap LED
  - Red Power Good LED (LED1)
  - Green FPGA DONE LED (LED2)
- Spartan-6 FPGA
  - Xilinx XC6SLX25T/75T/100T/150T-2
- Flash device is programmable via JTAG
- FPGA clock options:
  - Programmable clock generator (5 KHz – 500 MHz), three clock outputs connected to FPGA
  - Two differential reference clocks from FMC slot
- 2x DDR3 SDRAM bank, 64M x 16 (128 MB) each
- 64 Mbit SPI-EEPROM
- VITA 57.1 FMC slot (low pin count)
  - 68 single-ended or 34 differential I/O lines
  - 2 differential reference clocks
  - x1 multi-gigabit link
  - \( V_{\text{adj}} = 1.2 \) – 3.3 Volt
- Operating temperature -40°C to +85°C
- MTBF (MIL-HDBK217F/FN2 Gb 20°C)
  - TAMC631: 260 000 h

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e-mail: info@tews.com  www.tews.com

Issue 1.0.0  2013-11-13
The Embedded I/O Company

Order Information

RoHS Compliant

| TAMC631-10R       | Spartan-6 FPGA Module, Single Mid-Size, XC6SLX25T-2, 256 MB DDR3, FMC Slot |
| TAMC631-11R       | Spartan-6 FPGA Module, Single Full-Size, XC6SLX25T-2, 256 MB DDR3, FMC Slot |
| TAMC631-12R       | Spartan-6 FPGA Module, Single Mid-Size, XC6SLX75T-2, 256 MB DDR3, FMC Slot |
| TAMC631-13R       | Spartan-6 FPGA Module, Single Full-Size, XC6SLX75T-2, 256 MB DDR3, FMC Slot |
| TAMC631-14R       | Spartan-6 FPGA Module, Single Mid-Size, XC6SLX100T-2, 256 MB DDR3, FMC Slot |
| TAMC631-15R       | Spartan-6 FPGA Module, Single Full-Size, XC6SLX100T-2, 256 MB DDR3, FMC Slot |
| TAMC631-16R       | Spartan-6 FPGA Module, Single Mid-Size, XC6SLX150T-2, 256 MB DDR3, FMC Slot |
| TAMC631-17R       | Spartan-6 FPGA Module, Single Full-Size, XC6SLX150T-2, 256 MB DDR3, FMC Slot |

Optional available on request:
- Faster FPGA speed grades

For the availability of non-RoHS compliant (leaded solder) products please contact TEWS.

Documentation

| TAMC631-DOC       | User Manual                                      |
| TAMC631-ED        | Engineering Documentation for TAMC631, includes TAMC631-DOC, Data Sheets, Constraints Files |
| TAMC631-FDK       | FPGA Development Kit for TAMC631, includes TPLD001 Example Design |

Accessories

| TA900-10R         | Program and Debug Box, USB, JTAG, 20pin FPC connector, including USB A-USB B and FPC Flexcable |

Software

| TDRV015-SW-25     | Integrity Software Support (for the example design TPLD001 of the TAMC631-FDK) |
| TDRV015-SW-42     | VxWorks (Legacy and VxBus-Enabled) Software Support (for the example design TPLD001 of the TAMC631-FDK) |
| TDRV015-SW-65     | Windows Software Support (for the example design TPLD001 of the TAMC631-FDK) |
| TDRV015-SW-72     | LynxOS Software Support (for the example design TPLD001 of the TAMC631-FDK) |
| TDRV015-SW-82     | Linux Software Support (for the example design TPLD001 of the TAMC631-FDK) |
| TDRV015-SW-95     | QNX Software Support (for the example design TPLD001 of the TAMC631-FDK) |

For other operating systems please contact TEWS.
The Embedded I/O Company

TAMC640  Virtex-5 AMC with FMC Slot

Application Information

The TAMC640 is a standard single Mid-Size or Full-Size AMC module providing a user configurable Virtex-5 FPGA. The integrated PCIe Endpoint Block of the Virtex-5 can be used to build an x1, x4 or x8 PCIe link via AMC Port 4-11. The implementation of other protocols like SRIO or XAUI is also possible. AMC Ports 0 & 1, commonly used for Gigabit Ethernet, are also connected to the FPGA. The integrated Gigabit Ethernet MACs of the Virtex-5 allow fast and easy protocol implementation.

To allow direct board-to-board communication, AMC Ports 12-17 are connected to Virtex-5 I/Os, allowing AC-coupled LVDS communication with a port speed up to 1.0Gb/sec.

For flexible I/O solutions the TAMC640 provides a VITA 57.1 high pin count FMC Module slot, allowing active and passive signal conditioning. All FMC I/O lines are directly connected to the FPGA, which maintains the flexibility of the Select I/O technology of the Virtex-5 FPGA.

In addition, the FPGA is connected to the following external memories:

- 256MB DDR2 SDRAM, organized as two banks of 64 M x 16
- 2MB QDR-II SRAM, organized as one bank of 1 M x 18

Multiple clocks from the AMC-interface, the FMC and from on-board sources are supplied to the FPGA.

The FPGA is configured by a flash device, which is in-system programmable and able to store multiple code versions.

The TAMC640 supports encrypted FPGA bitstream usage. Encrypted FPGA bitstreams cannot be copied or reverse engineered, securing your intellectual property.

The IPMI Connectivity Records located inside the Module Management Controller (MMC) can be modified by the customer (e.g. via IPMI), to adapt to the different possible communication protocols (PCIe, SRIO, XAUI, ...).

User applications for the TAMC640 require the full ISE Foundation software, which must be purchased from Xilinx.

The Engineering Documentation TAMC640-ED includes all information needed for customer specific FPGA programming. The FPGA Development Kit TAMC640-FDK includes the engineering documentation, ucf-files with all necessary pin assignments and basic timing constraints, and a well documented VHDL example application. This example application is called TPLD002 (Tews Programmable Logic Design) and covers the main functionalities of the TAMC640 like DMA capable PCIe endpoint with interrupt support, register mapping, DDR2 and QDR-II memory access and basic I/O to the FMC slot. It comes as a Xilinx ISE project with source code and as a ready-to-download bitstream. It is the basis for fast and reliable customer application development, and can significantly reduce time to market.

Software support for the TPLD002 is available for all major operating systems.

In-circuit programming and debugging of the FPGA design (e.g. using Xilinx “ChipScope”) is supported. The Program and Debug Box TA900 allows access to the module while it is inserted in a system. It provides access to the module’s JTAG Chain, the UART of the on-board Module Management Controller (MMC) and to two user pins of the Virtex-5 FPGA. If a UART core is implemented in the FPGA, serial communication via the TA900 is possible.

The TA900 can be accessed by USB 2.0 and by a 14-pin JTAG Header (e.g. for connecting a Xilinx Platform Cable). For First-Time-Buyers the TA900 and the TAMC640-ED or TAMC640-FDK is recommended.
Technical Information

- Form Factor: PICMG AMC.0 R2.0 Module
  - Board size: single Mid-Size or Full-Size AMC
- AMC port 0,1 and 4 – 11 connected to FPGA MGTs
  - on-board AC-coupling for Rx and Tx
  - port speed up to 3.2Gb/sec
- AMC port 12 – 15 & 17 connected to FPGA I/Os
  - on-board AC-coupling for Rx and Tx
  - port speed up to 1.0Gb/sec
- TCLKA – TCLKD support
- Virtex-5 FPGA with integrated PCIe Endpoint Block
  - XC5VLX50T or XC5VLX85T
  - XC5VSX50T
- 2 MB QDR-II SRAM
  - 1 bank
  - 1 M x18
- 256 MB DDR2 SDRAM
  - 2 banks
  - 64 M x16 (128 MB) each
- IPMI V1.5 support
- Front panel LEDs:
  - Blue Hot Swap LED
  - Red FAIL LED (LED1)
  - Green USER / Power Good LED (LED2)
- VITA 57.1 FMC Slot (high pin count)
  - 160 single ended I/Os or 80 differential
  - x2 Multi-Gigabit Link to FMC
  - $V_{ADJ} = 1.2 – 3.3$ Volt
- Operating temperature 0°C to +70°C
- MTBF (MIL-HDBK217F/FN2 G8 20°C)
  - TAMC640: 306000 h

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2015-07-22
Order Information

RoHS Compliant

TAMC640-10R  Virtex-5 FPGA Module, Single Mid-Size, XC5VLX50T-1, 256 MB DDR3, 2 MB QDR-II, FMC Slot
TAMC640-11R  Virtex-5 FPGA Module, Single Full-Size, XC5VLX50T-1, 256 MB DDR3, 2 MB QDR-II, FMC Slot
TAMC640-12R  Virtex-5 FPGA Module, Single Mid-Size, XC5VLX85T-1, 256 MB DDR3, 2 MB QDR-II, FMC Slot
TAMC640-13R  Virtex-5 FPGA Module, Single Full-Size, XC5VLX85T-1, 256 MB DDR3, 2 MB QDR-II, FMC Slot
TAMC640-14R  Virtex-5 FPGA Module, Single Mid-Size, XC5VSX50T-1, 256 MB DDR3, 2 MB QDR-II, FMC Slot
TAMC640-15R  Virtex-5 FPGA Module, Single Full-Size, XC5VSX50T-1, 256 MB DDR3, 2 MB QDR-II, FMC Slot

Optional available on request:
- Operating temperature -40°C to +85°C
- Faster FPGA speed grades
- 512 MB DDR2 (2 banks 128 M x 16)
- 4 MB QDR-II (1 bank of 2 M x 18) or 8 MB QDR-II (1 bank of 4 MB x 18)

For the availability of non-RoHS compliant (lead solder) products please contact TEWS.

Documentation

TAMC640-DOC  User Manual
TAMC640-ED   Engineering Documentation for TAMC640, includes TAMC640-DOC, Data Sheets, Constraints Files
TAMC640-FDK  FPGA Development Kit for TAMC640, includes TPLD002 Example Design

Accessories

TA900-10R    Program and Debug Box, USB, JTAG, 20pin FPC connector, including USB A-USB B and FPC Flexcable

Software

TDRV015-SW-25  Integrity Software Support (for the example design TPLD002 of the TAMC640-FDK)
TDRV015-SW-42  VxWorks (Legacy and VxBus-Enabled) Software Support (for the example design TPLD002 of the TAMC640-FDK)
TDRV015-SW-65  Windows Software Support (for the example design TPLD002 of the TAMC640-FDK)
TDRV015-SW-72  LynxOS Software Support (for the example design TPLD002 of the TAMC640-FDK)
TDRV015-SW-82  Linux Software Support (for the example design TPLD002 of the TAMC640-FDK)
TDRV015-SW-95  QNX Software Support (for the example design TPLD002 of the TAMC640-FDK)

For other operating systems please contact TEWS.
Application Information

The TAMC641 is a standard single Mid-Size or Full-Size AMC module providing a user configurable Virtex-5 FPGA. The integrated PCIe Endpoint Block of the Virtex-5 can be used to build an x1, x4 or x8 PCIe link via AMC Port 4-11. The implementation of other protocols like SRI0 or XAUI is also possible. AMC Ports 0 & 1, commonly used for Gigabit Ethernet, and AMC Ports 2 & 3 are also connected to the FPGA. The integrated Gigabit Ethernet MACs of the Virtex-5 allow fast and easy protocol implementation.

To allow direct board-to-board communication, AMC Ports 12-17 are connected to Virtex-5 I/Os, allowing AC-coupled LVDS communication with a port speed up to 1.0Gb/sec.

For flexible I/O solutions the TAMC641 provides a VITA 57.1 high pin count FMC Module slot, allowing active and passive signal conditioning. All FMC I/O lines are directly connected to the FPGA, which maintains the flexibility of the Select I/O technology of the Virtex-5 FPGA.

In addition, the FPGA is connected to the following external memories:
- 512MB DDR2 SDRAM, organized as two banks of 64 M x 32
- 4MB QDR-II SRAM, organized as two banks of 1 M x 18

Multiple clocks from the AMC-interface, the FMC and from on-board sources are supplied to the FPGA.

The FPGA is configured by a flash device, which is in-system programmable and able to store multiple code versions.

The TAMC641 supports encrypted FPGA bitstream usage. Encrypted FPGA bitstreams cannot be copied or reverse engineered, securing your intellectual property.

The IPMI Connectivity Records located inside the Module Management Controller (MMC) can be modified by the customer (e.g. via IPMI), to adapt to the different possible communication protocols (PCIe, SRI0, XAUI, ...).

User applications for the TAMC641 require the full ISE Foundation software, which must be purchased from Xilinx.

The Engineering Documentation TAMC641-ED includes all information needed for customer specific FPGA programming. The FPGA Development Kit TAMC641-FDK includes the engineering documentation, ucf-files with all necessary pin assignments and basic timing constraints, and a well documented VHDL example application. This example application is called TPLD003 (Tews Programmable Logic Design) and covers the main functionalities of the TAMC641 like DMA capable PCIe endpoint with interrupt support, register mapping, DDR2 and QDR-II memory access and basic I/O to the FMC slot. It comes as a Xilinx ISE project with source code and as a ready-to-download bitstream. It is the basis for fast and reliable customer application development, and can significantly reduce time to market.

Software support for the TPLD003 is available for all major operating systems.

In-circuit programming and debugging of the FPGA design (e.g. using Xilinx "ChipScope") is supported. The Program and Debug Box TA900 allows access to the module while it is inserted in a system. It provides access to the module's JTAG Chain, the UART of the on-board Module Management Controller (MMC) and to two user pins of the Virtex-5 FPGA. If a UART core is implemented in the FPGA, serial communication via the TA900 is possible.

The TA900 can be accessed by USB 2.0 and by a 14-pin JTAG Header (e.g. for connecting a Xilinx Platform Cable).

For First-Time-Buyers the TA900 and the TAMC641-ED or TAMC641-FDK is recommended.
The Embedded I/O Company

Technical Information

- Form Factor: PICMG AMC.0 R2.0 Module
  - Board size: single Mid-Size or Full-Size AMC
- AMC port 0 – 11 connected to FPGA MGTs
  - on-board AC-coupling for Rx and Tx
  - port speed up to 3.2Gb/sec (6.5Gb/s for FX)
- AMC port 12 – 15 & 17 connected to FPGA I/Os
  - on-board AC-coupling for Rx and Tx
  - port speed up to 1.0Gb/sec
- TCLKA – TCLKD support
- Virtex-5 FPGA with integrated PCIe Endpoint Block
  - XC5VLX110T or XC5VLX155T
  - XC5VSX95T
  - XC5VFX70T or XC5VFX100T
- 4MB QDR-II SRAM
  - 2 banks
  - 1M x18 (2 MB) each

- 512 MB DDR2 SDRAM
  - 2 banks
  - 64 M x32 (256 MB) each
- IPMI V1.5 support
- Front panel LEDs:
  - Blue Hot Swap LED
  - Red FAIL LED (LED1)
  - Green USER / Power Good LED (LED2)
- Vita57.1 FMC Slot (high pin count)
  - 160 single ended I/Os or 80 differential
  - x4 Multi-Gigabit Link to FMC
  - V\text{\textsubscript{ADJ}} = 1.2 – 3.3 Volt
- Operating temperature 0°C to +70°C
- MTBF (MIL-HDBK217F/FN2 G\textsubscript{B} 20°C)
  - TAMC641: 304000 h

- 512 MB DDR2 SDRAM
  - 2 banks
  - 64 M x32 (256 MB) each
- IPMI V1.5 support
- Front panel LEDs:
  - Blue Hot Swap LED
  - Red FAIL LED (LED1)
  - Green USER / Power Good LED (LED2)
- Virtex-5 FPGA with integrated PCIe Endpoint Block
  - XC5VLX110T or XC5VLX155T
  - XC5VSX95T
  - XC5VFX70T or XC5VFX100T
- 4MB QDR-II SRAM
  - 2 banks
  - 1M x18 (2 MB) each

- 512 MB DDR2 SDRAM
  - 2 banks
  - 64 M x32 (256 MB) each
- IPMI V1.5 support
- Front panel LEDs:
  - Blue Hot Swap LED
  - Red FAIL LED (LED1)
  - Green USER / Power Good LED (LED2)
- Virtex-5 FPGA with integrated PCIe Endpoint Block
  - XC5VLX110T or XC5VLX155T
  - XC5VSX95T
  - XC5VFX70T or XC5VFX100T
- 4MB QDR-II SRAM
  - 2 banks
  - 1M x18 (2 MB) each

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Issue 1.0.1
2015-07-22
Order Information

RoHS Compliant

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<th>Code</th>
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<tbody>
<tr>
<td>TAMC641-10R</td>
<td>Virtex-5 FPGA Module, Single Mid-Size, XC5VLX110T-1, 512 MB DDR3, 4 MB QDR-II, FMC Slot</td>
</tr>
<tr>
<td>TAMC641-11R</td>
<td>Virtex-5 FPGA Module, Single Full-Size, XC5VLX110T-1, 512 MB DDR3, 4 MB QDR-II, FMC Slot</td>
</tr>
<tr>
<td>TAMC641-12R</td>
<td>Virtex-5 FPGA Module, Single Mid-Size, XC5VLX155T-1, 512 MB DDR3, 4 MB QDR-II, FMC Slot</td>
</tr>
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<td>TAMC641-13R</td>
<td>Virtex-5 FPGA Module, Single Full-Size, XC5VLX155T-1, 512 MB DDR3, 4 MB QDR-II, FMC Slot</td>
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<tr>
<td>TAMC641-14R</td>
<td>Virtex-5 FPGA Module, Single Mid-Size, XC5VSX95T-1, 512 MB DDR3, 4 MB QDR-II, FMC Slot</td>
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<tr>
<td>TAMC641-15R</td>
<td>Virtex-5 FPGA Module, Single Full-Size, XC5V SX95T-1, 512 MB DDR3, 4 MB QDR-II, FMC Slot</td>
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<tr>
<td>TAMC641-16R</td>
<td>Virtex-5 FPGA Module, Single Mid-Size, XC5VFX70T-1, 512 MB DDR3, 4 MB QDR-II, FMC Slot</td>
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<tr>
<td>TAMC641-17R</td>
<td>Virtex-5 FPGA Module, Single Full-Size, XC5VFX70T-1, 512 MB DDR3, 4 MB QDR-II, FMC Slot</td>
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<tr>
<td>TAMC641-18R</td>
<td>Virtex-5 FPGA Module, Single Mid-Size, XC5VFX100T-1, 512 MB DDR3, 4 MB QDR-II, FMC Slot</td>
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<tr>
<td>TAMC641-19R</td>
<td>Virtex-5 FPGA Module, Single Full-Size, XC5VFX100T-1, 512 MB DDR3, 4 MB QDR-II, FMC Slot</td>
</tr>
</tbody>
</table>

Optional available on request:
- Operating temperature -40°C to +85°C
- Faster FPGA speed grades
- 1 GB DDR2 (2 banks 128 M x 32)
- 8 MB QDR-II (2 banks of 2 M x 18) or 16 MB QDR-II (2 banks of 4 M x 18)

For the availability of non-RoHS compliant (leaded solder) products please contact TEWS.

Documentation

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</tr>
<tr>
<td>TAMC641-ED</td>
<td>Engineering Documentation includes TAMC641-DOC, Data Sheets, Constraints Files</td>
</tr>
<tr>
<td>TAMC641-FDK</td>
<td>FPGA Development Kit for TAMC641, includes TPLD003 Example Design</td>
</tr>
</tbody>
</table>

Accessories

<table>
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<th>Code</th>
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<tr>
<td>TA900-10R</td>
<td>Program and Debug Box, USB, JTAG, 20pin FPC connector, including USB A-USB B and FPC Flexcable</td>
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</table>

Software

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<tr>
<td>TDRV015-SW-25</td>
<td>Integrity Software Support (for basic example design TPLD003 of the TAMC641-FDK)</td>
</tr>
<tr>
<td>TDRV015-SW-42</td>
<td>VxWorks Software Support (for basic example design TPLD003 of the TAMC641-FDK, Legacy and VxBus-Enabled Software Support)</td>
</tr>
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<td>Windows Software Support (for basic example design TPLD003 of the TAMC641-FDK)</td>
</tr>
<tr>
<td>TDRV015-SW-72</td>
<td>LynxOS Software Support (for basic example design TPLD003 of the TAMC641-FDK)</td>
</tr>
<tr>
<td>TDRV015-SW-82</td>
<td>Linux Software Support (for basic example design TPLD003 of the TAMC641-FDK)</td>
</tr>
<tr>
<td>TDRV015-SW-95</td>
<td>QNX Software Support (for basic example design TPLD003 of the TAMC641-FDK)</td>
</tr>
</tbody>
</table>

For other operating systems please contact TEWS.
**Application Information**

The TAMC651 is a double Mid-Size or Full-Size AMC.1 Type 1 module according to MTCA.4 (MicroTCA Enhancements for Rear I/O and Precision Timing) and provides a user configurable Spartan-6 FPGA (XC6SLX45T-2 or XC6SLX100T-2).

The Spartan-6's integrated PCIe Endpoint Block is connected to AMC port 4.

AMC ports 12-15 (point-to-point) and AMC ports 17-20 (multi-drop) connect to FPGA I/O pins via on-board M-LVDS transceivers.

One of the Spartan-6 GTP transceivers utilizes an SFP interface available at the front plate. SFP support signals are available as FPGA I/O pins. Four FPGA controlled LEDs are also available at the front plate.

According to MTCA.4, the TAMC651 provides two 30-pair ADF connectors at the Zone 3 interface (Rear I/O).

The following I/O signals are available at the Zone 3 interface: 46 differential FPGA I/O lines (LVDS), 2 differential reference clock lines (LVDS), 2 Spartan-6 GTP transceivers. The differential FPGA I/O lines could also be used as single-ended I/O lines (FPGA bank supply for the Zone 3 I/O signals is 2.5V).

The TAMC651 provides a 128 Mbyte, 16 bit wide DDR3 SDRAM bank. The SDRAM-interface utilizes one of the internal hardwired Memory Controller Blocks of the Spartan-6 FPGA.

The FPGA is configured via a Xilinx platform flash which is programmable via a JTAG header. The JTAG header also supports readback and on-chip debugging of the FPGA design (e.g. using Xilinx "ChipScope"). A serial SPI-Flash can be used as alternative configuration data source or for user data storage.

The TAMC651 is shipped with blank configuration devices.

A programmable clock generator supplies differential clock lines to FPGA global clock pins, to an on-board clock crosspoint-switch and to the Spartan-6 GTP transceiver used for the SFP interface. The clock generator is programmable by the FPGA design.

The TAMC651 also provides a configurable clock crosspoint-switch. Clock inputs are: programmable clock generator output, FPGA clock output, AMC TCLKA and TCLKB. Two clock outputs are connected to FPGA global clock pins and two clock outputs are available as reference clocks at the Zone 3 interface.

User applications for the TAMC651 options with the XC6SLX45T-2 FPGA can be developed using the ISE WebPACK design software, which is available free of charge from www.xilinx.com. TAMC651 options with the XC6SLX100T-2 require a full licensed ISE Design Suite.

TEWS offers an FPGA Development Kit (TAMC651-FDK) which consists of a well documented basic example design. It includes an .ucf file with all necessary pin assignments and basic timing constraints. The example design covers certain functionalities of the TAMC651. It implements a DMA capable PCIe endpoint with interrupt support, register mapping and DDR3 memory access. It comes as a Xilinx ISE project with source code and as a ready-to-download bitstream.

Please note: The basic example design requires the Embedded Development Kit (EDK), which is part of the Embedded or System Edition of the ISE Design Suite from Xilinx (downloadable from www.xilinx.com, a 30 day evaluation license is available).

Software support for the basic design example of the TAMC651-FDK will be available for all major operating systems.

The TAMC651 can also be accessed via the TA900 program/debug box (USB 2.0 and/or 14-pin JTAG Header).

For First-Time-Buyers the TA900, the TAMC651-ED and TAMC651-FDK are recommended.
Technical Information

- Form Factor: PICMG AMC.0 Module
  - Double width
  - Mid-Size or Full-Size front panel
  - Front panel mechanics and Zone 3 interface according to MTCA.4
- PCIe x1 link (AMC.1 Type 1 compliant)
- M-LVDS transceivers for AMC ports 12-15 (point-to-point) and AMC ports 17-20 (multi-point)
- Spartan-6 FPGA
  - Xilinx XC6SLX45T-2 or XC6SLX100T-2
  - FPGA configuration options
  - Xilinx Platform Flash
  - SPI serial Flash
  - JTAG Header
- DDR3 SDRAM bank, 64M x 16 (128 MB)
- Front Panel LEDs:
  - Blue Hot-Swap LED
  - Red LED (LED1)
  - Green LED (LED2)
  - 4x user programmable LED
- IPMI V1.5 support
- Programmable Clock Generator
  - 2 clock lines to FPGA
  - 1 clock line to SFP/GTP transceiver
  - 1 clock line to Clock Crosspoint-Switch
- Clock Crosspoint-Switch
  - Inputs: Programmable Clock Generator Clock Output, TCLKA, TCLKB, FPGA Clock output
  - Outputs: 2 clock lines to FPGA, 2 clock lines to Zone 3 interface
- MTCA.4 Zone 3 Interface I/O
  - 46 differential I/O lines (LVDS), could also be used as single-ended I/O lines (FPGA bank supply 2.5V)
  - 2 differential reference clocks
  - 2 Spartan-6 GTP transceivers (μRTM provides the GTP reference clocks)
- 1x SFP Interface at the front plate
- Zone 3 mechanical Key N = 1 (LVDS)
# Order Information

## RoHS Compliant
- **TAMC651-10R**  Spartan-6 FPGA Module, Double Mid-Size, MTCA.4 I/O, XC6SLX45T-2, 128 MB DDR3, 1 x SFP Port
- **TAMC651-11R**  Spartan-6 FPGA Module, Double Full-Size, MTCA.4 I/O, XC6SLX45T-2, 128 MB DDR3, 1 x SFP Port
- **TAMC651-12R**  Spartan-6 FPGA Module, Double Mid-Size, MTCA.4 I/O, XC6SLX100T-2, 128 MB DDR3, 1 x SFP Port
- **TAMC651-13R**  Spartan-6 FPGA Module, Double Full-Size, MTCA.4 I/O, XC6SLX100T-2, 128 MB DDR3, 1 x SFP Port

Optional available on request:
- Faster FPGA speed grades

For the availability of non-RoHS compliant (leaded solder) products please contact TEWS.

## Documentation
- **TAMC651-DOC**  User Manual
- **TAMC651-ED**  Engineering Documentation for TAMC651, includes TAMC651-DOC, Data Sheets, Constraints Files
- **TAMC651-FDK**  FPGA Development Kit for TAMC651, includes TPLD004 Example Design

## Accessories
- **TA900-10R**  Program and Debug Box, USB, JTAG, 20pin FPC connector, including USB A-USB B and FPC Flexcable

## Software
- **TDRV015-SW-25**  Integrity Software Support (for the example design TPLD004 of the TAMC651-FDK)
- **TDRV015-SW-42**  VxWorks (Legacy and VxBus-Enabled) Software Support (for the example design TPLD004 of the TAMC651-FDK)
- **TDRV015-SW-65**  Windows Software Support (for the example design TPLD004 of the TAMC651-FDK)
- **TDRV015-SW-72**  LynxOS Software Support (for the example design TPLD004 of the TAMC651-FDK)
- **TDRV015-SW-82**  Linux Software Support (for the example design TPLD004 of the TAMC651-FDK)
- **TDRV015-SW-95**  QNX Software Support (for the example design TPLD004 of the TAMC651-FDK)

For other operating systems please contact TEWS.
Application Information

The TAMC863 is a standard single Mid-Size/Full-Size AMC.1 compliant module with four high speed serial data communication channels.

The serial communication controller is implemented in FPGA logic, along with a bus master capable PCI interface, guaranteeing long term availability with the option to implement additional functions in the future. The FPGA is connected to the PCI Express interface via a PCI Express to PCI bridge.

Each channel has a receive and a transmit FIFO of 512 long words (32 bit) per channel for high data throughput. Data transfer on the PCI bus is handled via TAMC863 initiated DMA cycles with minimum host/CPU intervention.

Several serial communication protocols are supported by each channel, such as asynchronous, isochronous, synchronous and HDLC mode.

A 14.7456 MHz oscillator provides standard asynchronous baud rates. An additional 24 MHz oscillator is provided for other baud rates. A 10 MHz oscillator is used for the synchronous baud rate of 10 Mbit/s.

Each channel also provides various interrupt sources, generated on INTA. The interrupt sources can be enabled or disabled individually.

Multiprotocol transceivers are used for the line interface. The physical interface is selectable by software, individually for each channel as EIA-232, EIA-422, EIA-449, EIA-530, EIA-530A, V.35, V.36 or X.21.

The following signals are provided by the TAMC863 for each channel at the front I/O connector: Receive Data (RxD +/-), Transmit Data (TxD +/-), Receive Clock (RxC +/-), Transmit Clock (TxC +/-), Ready-To-Send (RTS +/-), Clear-To-Send (CTS +/-), Carrier-Detect (CD +/-) and GND. Additionally, serial channel 3 provides Data-Set-Ready (DSR3 +/-) and Data-Terminal-Ready (DTR3 +/-).

Technical Information

- Form Factor: PCIMG AMC.1 Module
- Board size: 180.6 mm x 73.5 mm
- Single Mid-Size / Full-Size
- PCIe single lane (x1) port (AMC.1 Type 1 compliant)
- IPMI Support
- Front Panel LEDs:
  - Blue Hot-Swap LED
  - Red Failure LED (LED1)
  - Green Power Good LED (LED 2)
- Four high speed synchronous/asynchronous serial interfaces
- Support of RxD, TxD, RxC, TxC, RTS, CTS, CD and GND on front connector, DTR3 and DSR3 on channel 3 only
- Physical interface (individually programmable per channel): EIA-232, EIA-422, EIA-449, EIA-530, EIA-530A, V.35, V.36 and X.21
- Maximum data rate: 10 Mbit/s (synchronous), 2 Mbit/s (asynchronous), internal or external provided clock
- EIA-232: up to 115.2 kbit/s
- Temperature range: -40°C to +85°C
Order Information

RoHS Compliant
TAMC863-10R  4 Ch. High Speed Synch/Asynch Serial Interface, Single Mid-Size
TAMC863-11R  4 Ch. High Speed Synch/Asynch Serial Interface, Single Full-Size

For the availability of non-RoHS compliant (leaded solder) products please contact TEWS.

Documentation
TAMC863-DOC  User Manual

Software
TDRV009-SW-25  Integrity Software Support
TDRV009-SW-42  VxWorks Software Support (Legacy and VxBus-Enabled Software Support)
TDRV009-SW-65  Windows Software Support
TDRV009-SW-72  LynxOS Software Support
TDRV009-SW-82  Linux Software Support
TDRV009-SW-95  QNX Software Support

For other operating systems please contact TEWS.

Related Products
TA307  Cable Kit for Modules with VHD68 Connector
The Embedded I/O Company

TAMC890  16 Port Gigabit Ethernet Switch

**Application Information**
The TAMC890 is a standard single width Mid-Size / Full-Size AMC.2 compliant 16 Port gigabit Ethernet Switch.
The TAMC890 supports four RJ45 front panel ports which are compliant to IEEE 802.3ab for 10BaseT, 100BaseTX and IEEE 802.3ab for 1000BaseT via CAT5 TP cable and 12 1.25G-SerDes/SGMII ports which are connected to the AMC backplane connector.
The TAMC890 is AMC.2 Type E2 and Type 4 compliant.
The auto-sensing and auto-negotiation function detect and configure automatically the data rate and the duplex mode.
The functionality of the TAMC890 based on the unmanaged Broadcom BCM5396 Gigabit Ethernet switch.
Front panel RJ45 ports are galvanically isolated from the transceiver and switch.
Each channel provides a front panel LEDs to indicate the different network activities.
The operating temperature range is 0°C to +70°C.

**Technical Information**
- Form Factor: PCIMG AMC.1 Module
  - Board size: 180.6mm x 73.5mm
  - Single width
  - Mid-Size/Full-Size front panel
- Fabric Interface:
  - AMC.2 Type E2 and Type 4 Interface
  - 6 additional GbE Ports on AMC port 12-15, 17 and 18
- IPMI V1.5 Support
- Front Panel LEDs:
  - Blue Hot-Swap LED
  - Red Fail LED (LED1)
  - Green Power LED (LED 2)
  - 16 x Link / Status LED
- 4 front panel RJ45 connectors
- 16-Channel 10/100/1000BaseTX Ethernet-Switch Broadcom BCM5396
  - Auto-Sensing und Auto-Negotiation
  - Integrated address management
  - 9KB Jumbo Frames
  - 4K VLAN
- Operating temperature 0°C to +70°C
- MTBF (MIL-HDBK217F/FN2 Gb 20°C)
  TAMC890: 5240000h

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Issue  1.0.0  2013-11-14
Order Information

RoHS Compliant

**TAMC890-10R** 16-Ch. Gigabit Ethernet-Switch, BCM5396, Single Mid-Size, 4 x RJ45, 12 x 1.25G-SerDes/SGMII on AMC connector

**TAMC890-11R** 16-Ch. Gigabit Ethernet-Switch, BCM5396, Single Full-Size, 4 x RJ45, 12 x 1.25G-SerDes/SGMII on AMC connector

For the availability of non-RoHS compliant (leaded solder) products please contact TEWS.

Documentation

**TAMC890-DOC** User Manual

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Issue 1.0.0 2013-11-14
**Application Information**

The TAMC900 is a high speed, high performance analog to digital converter AdvancedMC. In addition to the eight high speed ADCs, it provides excessive preprocessing power by a Virtex-5 FPGA and high speed on board memory for e.g. full bandwidth snapshots.

A Virtex-5 LX30T is assembled on the TAMC900-10R. The TAMC900-25R is assembled with a Virtex-5 SX35T. AMC Port 4-11 on the TAMC900-10R or Port 0, 1 and 4-9 on the TAMC900-25R can be used to transmit the ADC data to the CPU.

To adapt the TAMC900 to different customer requirements, the TAMC900 is equipped with a Signal Conditioning Adapter (SiCA) that contains the front panel with the connectors for the analog inputs, clock and trigger inputs and the analog signal conditioning.

The TAMC900 provides three clock inputs and three trigger inputs. The three external clock inputs and the PCIe reference clock are routed to a flexible clocking scheme that allows independent clocking of the ADCs in two groups. The trigger inputs are routed to the FPGA. Eight LTC2254 ADCs provide up to 105 MSps and 14 bit resolution each. The minimum sample rate is 1 Msp.s.

4 MByte high speed on board QDR-II SRAM enables snapshots of all ADCs at full speed and full resolution for 2ms.

According to AMC.0, the TAMC900 provides an IPMI compliant Module Management Controller (MMC) with temperature monitoring and hot-swap support.

The TAMC900 is delivered with a basic firmware, which allows gathering ADC data from all channels, triggering, clock configuration, and uses a PCIe x4 Link (AMC Port 4-7) to transmit ADC data to the CPU. Driver and Example Application for the basic firmware are available for different operating systems.
The Embedded I/O Company

Technical Information

- **Form Factor:** PCIMG AMC.0
- **Board size:** 180.6 mm x 73.5 mm
- **Single width / Mid-Size**
- **Fabric Interface:**
  - TAMC900-10R: Port 4-11
  - TAMC900-25R: Port 0-1 & 4-9
- **Virtex-5 FPGA**
  - TAMC900-10R: LX30T
  - TAMC900-25R: SX35T
- **4 MByte QDR-II SRAM**
- **IPMI Support**
- **Front Panel LEDs:**
  - Blue Hot-Swap LED
  - Red FAIL LED (LED1)
  - Green User LED (LED 2)
- **Analog-to-Digital Converter:**
  - 8 x LTC2254 ADCs
  - 105 MSps
  - 14 bit
  - 3 external clock inputs
  - 3 external trigger inputs
  - Signal Conditioning Adapter for flexible adoption to customer analog input requirements
- **Operating temperature:** 0°C to +55°C
**Order Information**

**RoHS Compliant**

<table>
<thead>
<tr>
<th>Product Code</th>
<th>Description</th>
<th>Features</th>
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</thead>
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<tr>
<td>TAMC900-10R</td>
<td>8 Ch. 14 Bit 105 MSps ADCs, Virtex-5 XC5VLX30T, 2 x 2 MB QDR-II, AMC port 4-11, requires TAMC900-A1</td>
<td></td>
</tr>
<tr>
<td>TAMC900-25R</td>
<td>8 Ch. 14 Bit 105 MSps ADCs, Virtex-5 XC5VLX35T, 2 x 2 MB QDR-II, AMC port 0,1 and 4-9, requires TAMC900-A1</td>
<td></td>
</tr>
<tr>
<td>TAMC900-A1-10R</td>
<td>Signal Conditioning Adapter for TAMC900, Gain = 1, Single Mid-Size</td>
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<tr>
<td>TAMC900-A1-11R</td>
<td>Signal Conditioning Adapter for TAMC900, Gain = 1, Single Full-Size</td>
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</tbody>
</table>

Optional available on request:
- Other FPGA (LX50T, SX50T, FX30T or FX70T)
- 8 MB QDR-II memory
- ADCs with different sample rate and resolution

For the availability of non-RoHS compliant (leaded solder) products please contact TEWS.

**Documentation**

<table>
<thead>
<tr>
<th>Product Code</th>
<th>Description</th>
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<tr>
<td>TAMC900-DOC</td>
<td>User Manual for TAMC900</td>
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**Software**

<table>
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<tr>
<th>Product Code</th>
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</thead>
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<tr>
<td>TAMC900-SW-25</td>
<td>Integrity Software Support (for basic firmware)</td>
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<tr>
<td>TAMC900-SW-42</td>
<td>VxWorks Software Support (for basic firmware)</td>
</tr>
<tr>
<td>TAMC900-SW-65</td>
<td>Windows Software Support (for basic firmware)</td>
</tr>
<tr>
<td>TAMC900-SW-72</td>
<td>LynxOS Software Support (for basic firmware)</td>
</tr>
<tr>
<td>TAMC900-SW-82</td>
<td>Linux Software Support (for basic firmware)</td>
</tr>
<tr>
<td>TAMC900-SW-95</td>
<td>QNX Software Support (for basic firmware)</td>
</tr>
</tbody>
</table>

For other operating systems please contact TEWS.
Application Information

The TA900 is an Interface Box which can be used to program and debug hardware modules providing a corresponding connector.

The Interface Box connects to compatible modules via a 20-pin Flexible Printed Circuit (FPC) Connector which can provide access to the module's JTAG Chain and the additional interfaces A and B.

The TA900 can be accessed by USB 2.0 and by a 14-pin JTAG Header, and is equipped with a Pushbutton Switch which is offering the possibility to send an impulse to one of the connected module's I/O pins.

A green LED indicates the assertion of this impulse by interrupting illumination.

In case of the user programmable FPGA boards TMC631 and TMC640/641, Interface A provides access to the UART of the onboard Module Management Controller (MMC), and Interface B connects to two user pins of the module’s onboard FPGA. If a UART core is implemented in the module's FPGA, serial communication via Interface B is possible.

By setting DIP Switches, the provided yellow LEDs located in the TA900 front panel can either indicate the logic level of the Interface's lines or can be configured to visualize serial communication on the Rx and Tx lines, if they are connected to the UART interfaces of the USB Controller.

Level Shifters can handle I/O voltages between 1.2V and 3.3V at the FPC Connector which offers a wide range of possible configurations for Interface A, B and the JTAG Chain of the connected hardware module.
The JTAG Chain of the connected hardware module which is useful to program and debug onboard devices can be accessed in two different ways:

If it is accessed via the 14-pin Header, which must be the case when communicating with Xilinx Devices, a "Xilinx Platform Cable USB II" (which is required) can be connected without any adaption.

If the JTAG Chain is accessed via the USB interface, Channel A of the USB Controller is not used to communicate with Interface A, but to generate JTAG signals for debugging or programming reasons. In this configuration, Lattice Devices for example can directly be programmed without the necessity of an additional Programming Cable, as the TA900 is directly supported by Lattice's Software Tool "ispVM".

The TA900 is self-powered by the FPC Connector which means that it is not necessary to connect the Interface Box to USB to provide a supply voltage.

The Interface Box meets the requirements to operate in extended temperature range from -30° to +75°C and comes with a **USB A to USB B Cable** and an **FPC Flexcable**.

**Technical Information**

- Form Factor: Interface Box
- Size: 139.7mm x 82.6mm x 26.2mm
- 20-pin Flexible Printed Circuit (FPC) Connector
- JTAG Interface
- Interface A (UART / MPSSE Mode JTAG)
- Interface B (UART)
- User I/O pin **BUTTON**
- I/O Voltages: 1.2V to 3.3V
- FTDI Chip FT2232H USB to UART/JTAG Controller
- Supported by "Lattice ispVM"
- USB B Receptacle
- USB 2.0 High Speed and Full Speed
- Self-Powered
- 14-pin Shrouded JTAG Header
- Matches the "Xilinx Platform Cable USB II" pinout
- Operating temperature -30°C to +75°C
- MTBF (MIL-HDBK217F/FN2 G= 20°C) TA900-10R: 639000 h
Order Information

RoHS Compliant
TA900-10R  Program and Debug Box, USB, JTAG, 20pin FPC connector, including USB A-USB B and FPC Flexcable

For the availability of non-RoHS compliant (leaded solder) products please contact TEWS.

Documentation
TA900-DOC  User Manual
FMC Modules

The FMC (FPGA Mezzanine Card) Mezzanine Modules conform to the ANSI/VITA 57.1 standard, and provide I/O modularity for FPGA processing devices on FMC Carrier Cards.

The need for different front panel I/O functionality within systems is constantly increasing. Typically, this front panel I/O functionality is fixed on 3U or 6U form factor cards. In practice, this means that if you want to change the front panel I/O functionality you have to replace the entire 3U or 6U card. Partial solutions are available with PMC and XMC Mezzanine Modules that provide configurable front panel I/O for 3U and 6U form factor carrier cards, but these still use most of the 3U and 6U carrier card area.

FMCs are new I/O mezzanine modules which connect to, but which are not limited to, 3U and 6U form factor cards. FMC Mezzanine Modules use a smaller and more modular form factor compared with PMC or XMC mezzanines. They are usually connected to an FPGA device or other device with a reconfigurable I/O capability. For example, they may be used on an AMC (Advanced Mezzanine Card) Carrier Card with an FMC site and FPGA for maximum flexibility.

FPGAs provide high pin count interfaces that are able to operate at high data rates up to multiple Gb/s. The state-of-the-art FMC Connector is able to maintain the high performance interface from the FPGA on the carrier card to the I/O on the FMC mezzanine module.

The FMC concept offers versatile modular I/O solutions, which can be used in various applications, environments, and markets. If necessary, double-width modules are available for applications that need additional FPGA carrier card bandwidth, greater front panel space, or a larger PCB area. Additionally, the FMC standard defines a commercial grade mezzanine module and a ruggedized conduction cooled variant.

To inquire about custom FMC designs, please contact TEWS directly at our offices in Germany or the United States. TEWS works closely with OEM and government customers to deliver accelerated time-to-market, long-term product availability and comprehensive product lifecycle management -- from the design stage through manufacturing, testing and beyond to post-sales support. For more information go to www.tews.com.
**Application Information**

The TFMC684 is an FMC (FPGA Mezzanine Card) Mezzanine Module complying with the ANSI/VITA 57.1 standard that offers the possibility to add a 32bit M-LVDS (Multipoint Low Voltage Differential Signaling) I/O Interface to FMC Carrier Cards.

The Low Pin Count FMC Connector provides 32 independent control signals which configure the direction of each M-LVDS Line Driver/Receiver.

The 32 data lines are routed as single-ended traces from the FMC Connector to the M-LVDS Transceivers where they are converted into 32 differential pairs meeting the TIA/EIA-899 standard (Type-2 Receivers). The 32 bits of differential I/O are connected to a VHDCI-68 Connector in the front panel.

On every of the 32 bits the TFMC684 supports signaling rates up to 200Mbit/s which means that a 100MHz clock can be transmitted or in other words that 200M of voltage transitions per second can be performed.

All signals connecting the M-LVDS Driver/Receivers with the FMC Carrier are powered by an adjustable voltage generated by the Carrier. Because of voltage translation devices on the TFMC684 this voltage can range from 1.2V to 3.6V which allows the FPGA's I/O cells to be configured for various different I/O standards.

The signaling standard reference voltage pin, which is powered by the TFMC684, provides half of the adjustable voltage generated by the carrier for I/O standards requiring a reference voltage.

A power good LED indicates whether all voltages on the TFMC684, which are provided by the FMC Carrier, are within limits.

The TFMC684 is equipped with an I²C EEPROM which acts as an IPMI resource requesting the value of the adjustable voltage, for example.

The module meets the requirements to operate in extended temperature range from -40° to +85°C.
Technical Information

- Form Factor: Single-width 10 mm stacking height
  FPGA Mezzanine Card (FMC) Mezzanine Module conforming to ANSI/VITA 57.1
  - Board size: 76.5 mm x 69 mm
  - Air cooled Commercial Grade with Front Panel
  - Regions 1 and 2 populated
- Low Pin Count (LPC) FMC Connector
- The 32 differential M-LVDS TIA/EIA-899 signals (up to 200Mbit/s each) are accessible at a VHDCI-68/SCSI-V female front I/O connector
  - VADJ can range from 1.2V to 3.6V
  - Direction of every bit is configurable independently
  - On-board EEPROM contains IPMI hardware definition
  - Operating temperature -40°C to +85°C
  - MTBF (MIL-HDBK217F/FN2 G6 20°C) TFMC684-10R: 873000 h

Order Information

RoHS Compliant
TFMC684-10R  32 Ch. M-LVDS, LPC-FMC, VHD68 connector

For the availability of non-RoHS compliant (leaded solder) products please contact TEWS.

Documentation
TFMC684-DOC  User Manual
Application Information

The TFMC900 is an FMC (FPGA Mezzanine Card) Mezzanine Module designed to test ANSI/VITA 57.1 FMC Carriers during development or series production. Additionally, it offers the possibility to realise various I/O solutions for connected FMC Carriers.

Interconnection of the High Pin Count FMC Connector signals can be verified by JTAG and by functional tests. A loop-back of the 10 multi-gigabit transceiver interfaces allows interconnection checks for the high-speed serial interfaces.

All voltages on the TFMC900 generated by the FMC Carrier are measured by Analog-to-Digital Converters which transfer the results via the JTAG interface.

The user configurable on-board Spartan-II FPGA, which is connected to the FMC Connector User Defined Signals and to a 68-pin Front I/O Connector, can be used to implement different I/O interfaces for the connected FMC Carrier.

The FPGA is connected to a Platform Flash to store configuration data which is accessible via the JTAG chain.

The TFMC900 is delivered with a blank configuration device. FPGA applications can be developed using the design software ISE WebPACK which can be downloaded free of charge at http://www.xilinx.com.

The FMC Connector User Defined Signals of Bank A are powered by an adjustable voltage generated by the Carrier which is preset to 3.3V (LVTTL) by IPMI. This voltage can be reduced to 2.5V (LVCMOS2) by changing the IPMI resource data inside the on-board I²C EEPROM for FPGAs not supporting the LVTTL signaling standard.

The voltage pins powering the I/O Bank B are connected to 2.5V generated by the FMC Mezzanine Module.

The TFMC900 generates six LVDS reference clock pairs and distributes them to the FMC Carrier. The frequency (common for all clock pairs) is adjustable by three dip switches on board.

The module meets the requirements to operate in extended temperature range from -40° to +85°C.
Technical Information

- Form Factor: Single-width 10 mm stacking height FPGA Mezzanine Card (FMC) Mezzanine Module conforming to ANSI/VITA 57.1
  - Board size: 84 mm x 69 mm
  - Air cooled Commercial Grade with Front Panel
  - Regions 1, 2 and 3 populated
- High Pin Count (HPC) FMC Connector
- 10 differential MGT interfaces are looped-back
- ADC with JTAG Interface to measure voltages
- Reconfigurable Spartan-II FPGA with Platform Flash
  - 40 MHz Clock
  - 68+48 FMC Bank A signals powered by VADJ
  - 44 FMC Bank B signals powered by 2.5V
- VREF_A_M2C, VREF_B_M2C and RES0 powered by VADJ
- Both VIO_B_M2C pins powered by 2.5V
- GA0, GA1, PG_M2C and PG_C2M powered by 3.3V
- 60 Front I/O signals powered by 3.3V
- The 60 Front I/O LVTTL signals at the VHDCI68/SCSI-V Connector are 5V tolerant
- On-board EEPROM contains IPMI hardware definition
- 2.5V I/O voltage for Bank B provided to the Carrier
- Adjustable differential clock generator
- Operating temperature -40°C to +85°C
- MTBF (MIL-HDBK217F/FN2 GB 20°C) TFMC900-10R: 655000 h

Order Information

RoHS Compliant
TFMC900-10R Test FMC, test ANSI/VITA 57.1 FMC Carriers during development or series production, HPC-FMC, VHD68 connector

For the availability of non-RoHS compliant (leaded solder) products please contact TEWS.

Documentation
TFMC900-DOC User Manual